REMARKS/ARGUMENTS

This is responsive to the Office Action dated July 12, 2004. The applicants acknowledge with appreciation the Examiner's allowance of claims 1-4 and 12-14. Further, the Examiner found allowable subject matter in claims 7-10, which if necessary will be made independent from any rejected claim by rewriting claim 7 in independent form. Accordingly, claims 1-4, 7-10 and 12-14 are in condition for allowance.

Claims 5, 6, 11 and 15-20 were all rejected as being anticipated by Edlund.

Claim 5 is being amended and reconsideration is requested. Claim 5 is supported at least by Figures 5A, 6 and 7 and the corresponding text. As amended, claim 5 is as follows:

> A synchronous rectifier comprising a power MOS device having a drain, a source and a gate, and an amplifier driving the gate of the power MOS device, the amplifier having a ~~first~~ positive input coupled to the ~~drain or~~ source of the power MOS device and a ~~second~~ negative input coupled to a reference voltage coupled between the ~~second~~ negative input and the ~~other of the~~ drain ~~or source~~ of the power MOS device whereby when the drain-source voltage across the ~~MOSFET~~ MOS device is near the reference voltage, the amplifier maintains the drain-source voltage at the reference voltage until the gate-source voltage equals approximately zero, thereby enabling zero current detection by an offset comparator.

Note specifically that claim 5 recites that the negative input of the amplifier is "coupled to a reference voltage coupled between the negative input and the drain of the power MOS device. According to the arrangement described in this claim, the reference voltage is connected to the drain of the MOS device and the negative input of the amplifier, which results in the operation set forth in the last four lines of claim 5. In contrast, refer to Figure 2 in Edlund. The Examiner is apparently referring to either B1 or B2 as being the reference voltage. Although both of these voltage sources are coupled to the negative input to the amplifier 30, neither of these voltage sources is coupled to the drain (or the source) of the MOS device, as claimed in claim 5. Even if modified to include another voltage source as set forth in Edlund's col. 4, lines 60-67, claim 5

would not be satisfied. Therefore, the anticipation rejection of claim 5 is requested to be withdrawn.

Referring now to claim 6, this claim is readable at least on Figure 3 and the corresponding text. Claim 6 recites a method wherein the apparent Rdson of the MOSFET is increased when the drain-source current is below a threshold level, thereby enabling zero crossing detection for improving performance of the MOSFET as a synchronous rectifier. In the embodiment of Figure 3, this method is performed by providing a main, larger MOSFET 200A with a relatively lower Rdson, and a smaller device 200B with a relatively higher Rdson. At low values of Id, the device 200B is turned on, providing a relatively higher Rdson. Page 4, lines 8-11. At higher values of Id, the main device 200A is also turned on, thereby providing a relatively lower Rdson. No such structure is present or function is performed in the device illustrated in Edlund and therefore it is not understood, or explained in the Office Action, how the method steps recited in claim 6 can be anticipated by the reference. There is no *prima facie* basis for a rejection.

Referring now to claim 11 which depends from claim 6, this claim indicates that the apparent drain source on resistance (Rdson) is increased by providing an offset voltage to maintain the drain-source voltage substantially constant until the gate-source voltage is approximately zero. Again, the Examiner apparently refers to the voltage sources B1 and B2 as providing an offset voltage. He may also be aware of Edlund's col. 4, lines 60-67. However, as mentioned above in connection with claim 5, the voltage sources B1 and B2 are not connected to a main terminal of the MOSFET as described and shown in this patent application, and the structures and functions of claim 6 are also absent, and therefore it is not understood, nor explained in the Office Action, how the method step of claim 11 can be anticipated by the reference. There is no *prima facie* basis for a rejection.

Referring now to claim 15, this claim, like claim 5, refers to "a reference voltage coupled between the negative input and the drain of the power MOS device." As explained above in connection with claim 5, the voltage sources B1 and B2, even if supplemented as described at col. 4, lines 60-67, are connected to one of the inputs of the amplifier but not to the terminals set forth in claim, the MOS device 28 therefore claim 15 is not anticipated.

Claim 16 has been amended to recite elements disclosed in Fig. 6 and is related to claim 19. Claim 17 has been rewritten in independent form. Claim 18 has been canceled and combined with its respective dependent claims 19 and 20. New claim 21 is related to claim 20. The reference and the Office Action fail to state a *prima facie* basis for rejection of claims16-17 and 19-21.

New dependent claims 22 and 23 depend respectively from claims 5 and 15.

In view of the foregoing, allowance of claims 1-17 and 19-23 is requested.

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